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FIG. 1

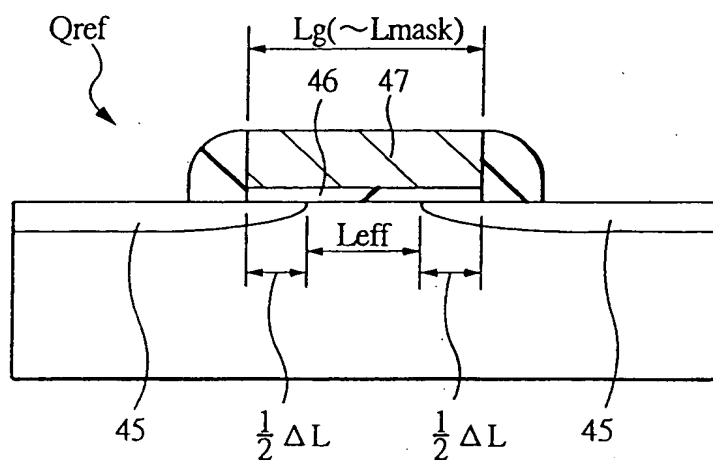
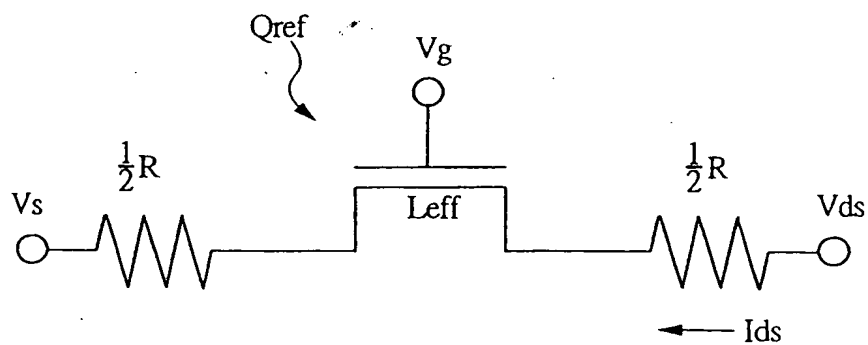
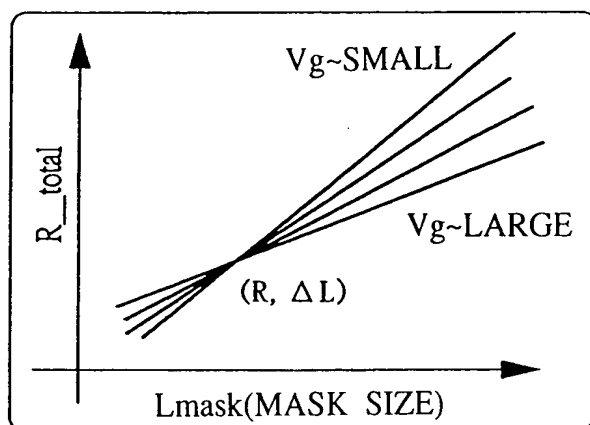
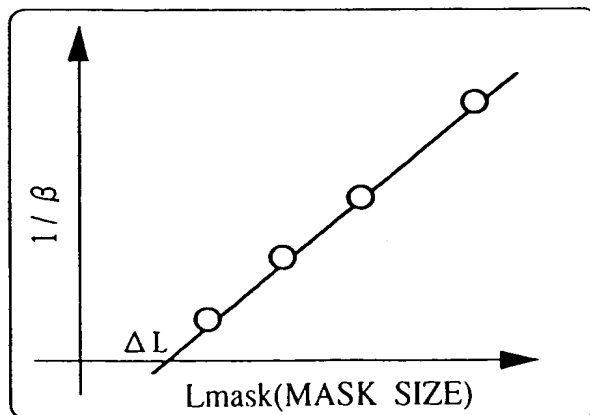
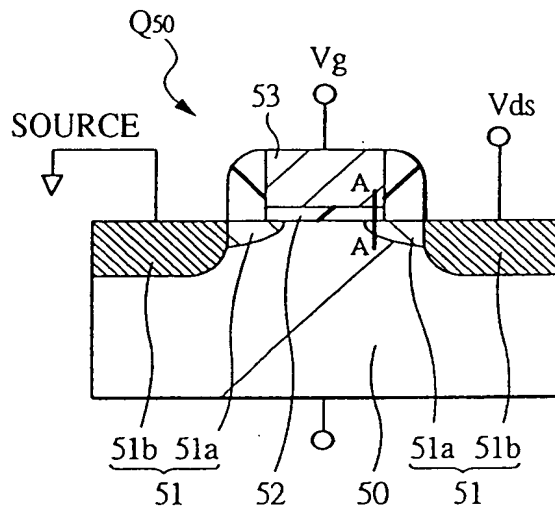


FIG. 2



*FIG. 3**FIG. 4*

**FIG. 5**



**FIG. 6(a)   FIG. 6(b)   FIG. 6(c)**

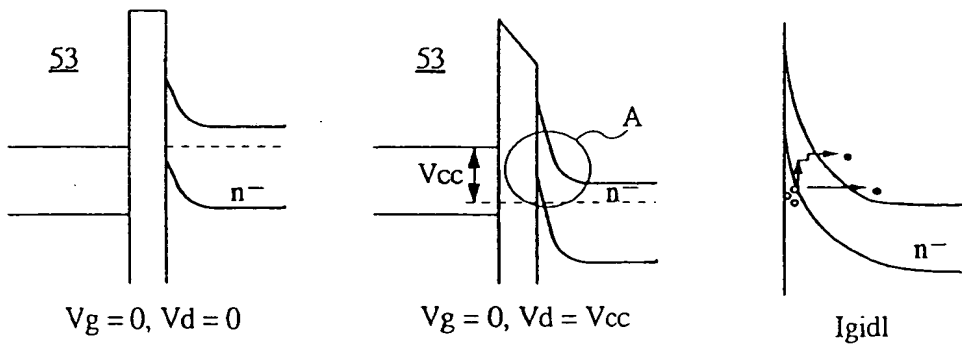


FIG. 7

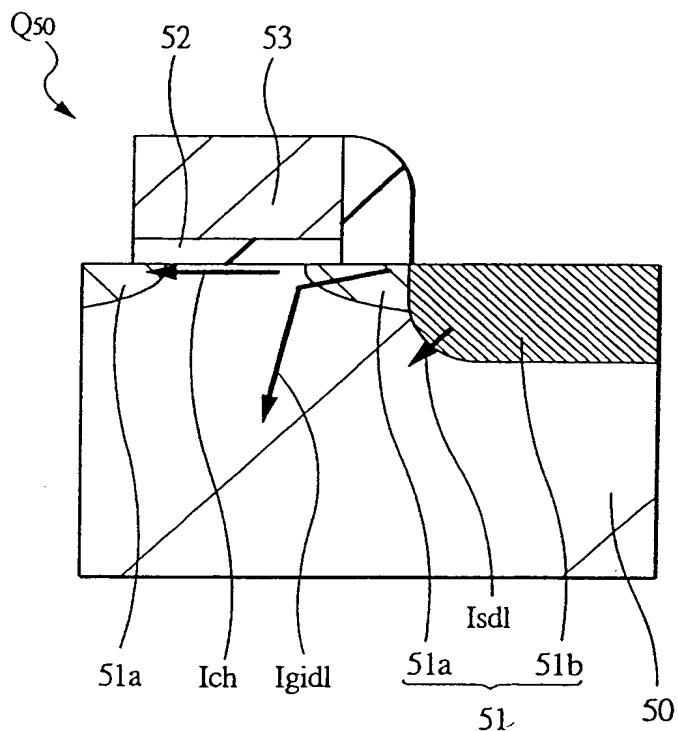
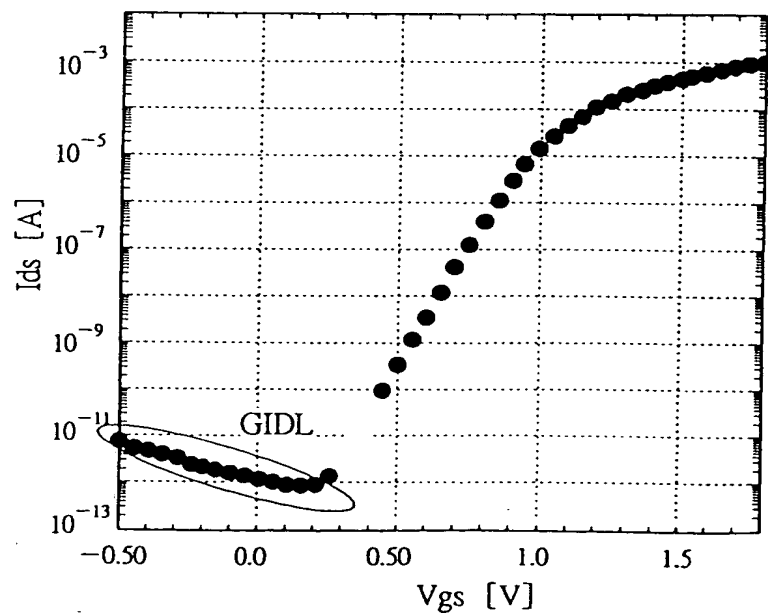


FIG. 8



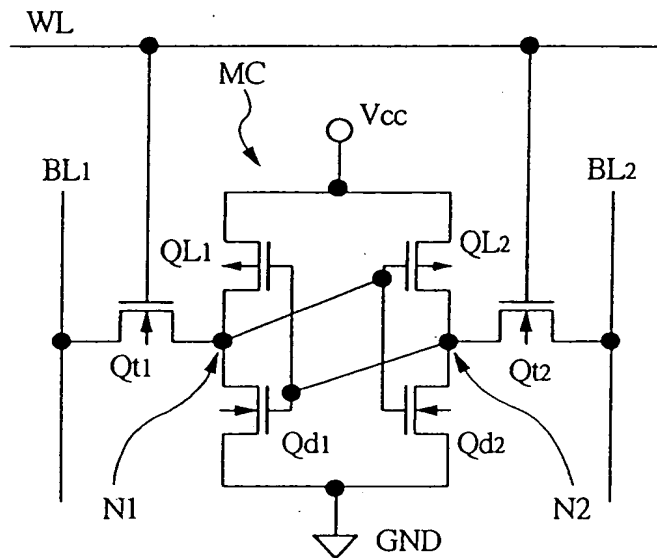
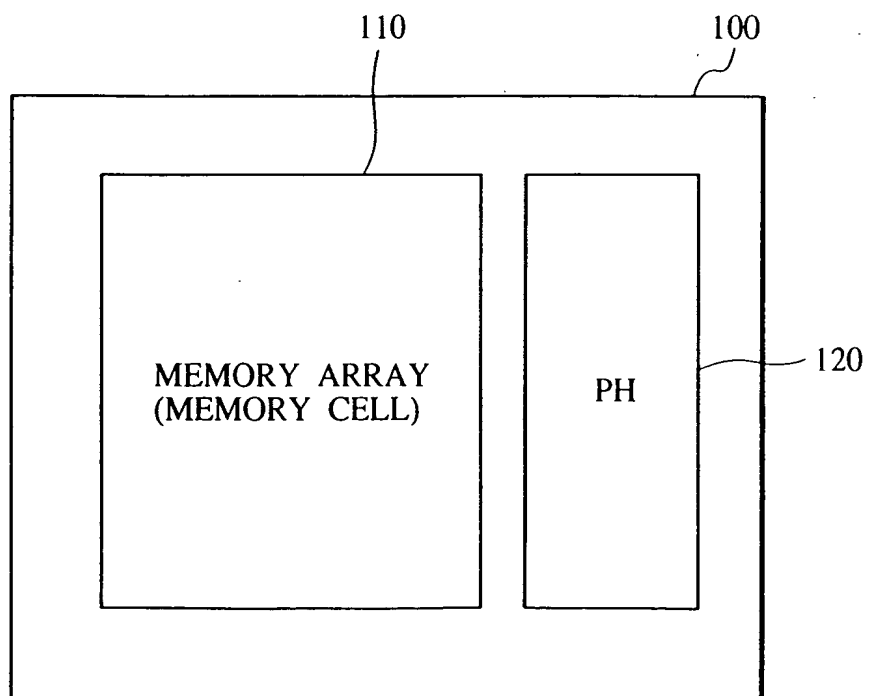
*FIG. 9(a)**FIG. 9(b)*

FIG. 10(a)

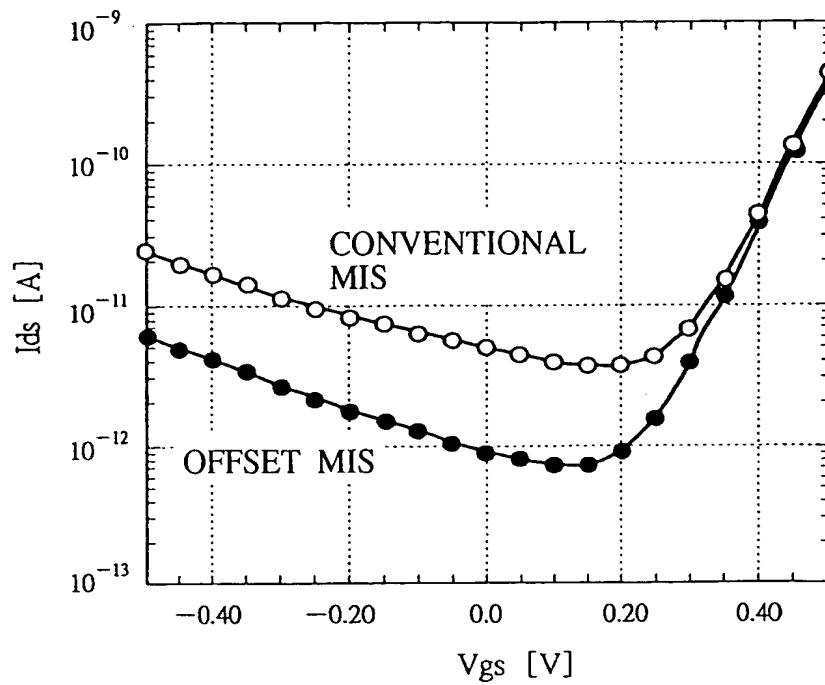
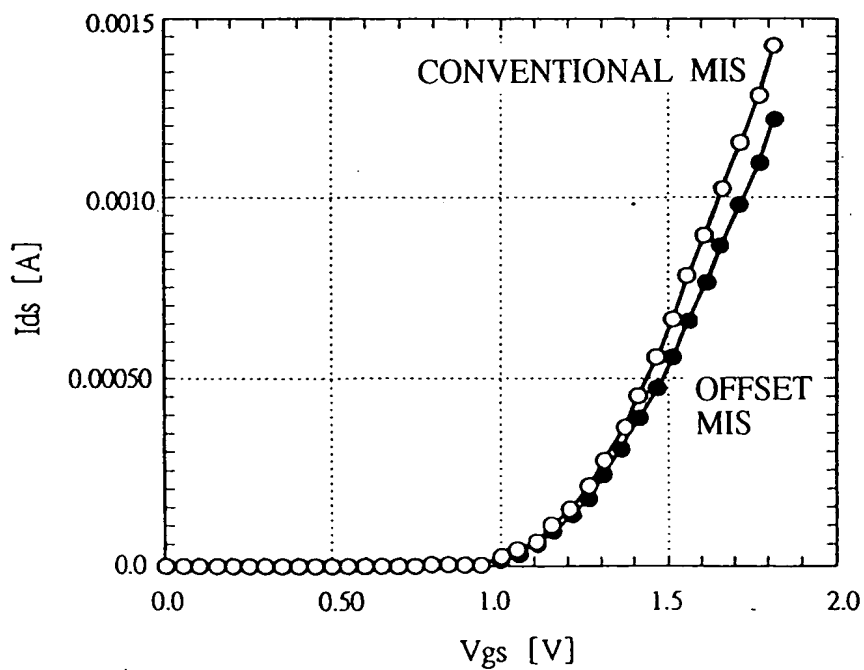


FIG. 10(b)



C. C.



C. C.





*FIG. 13*

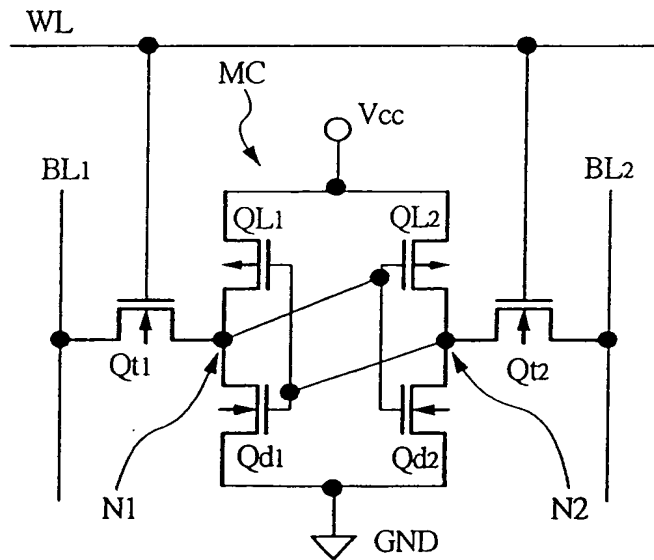


FIG. 14

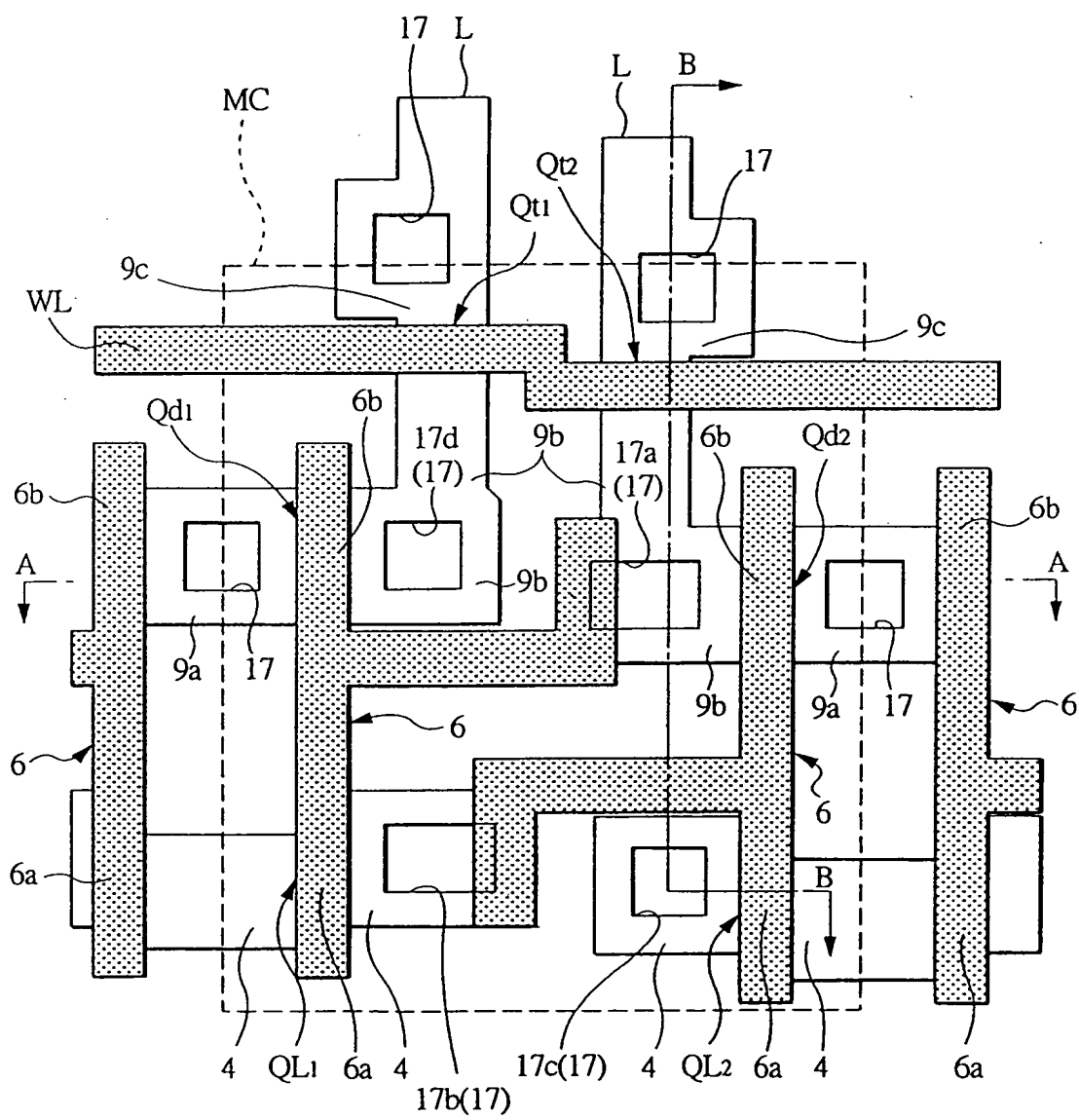


FIG. 15

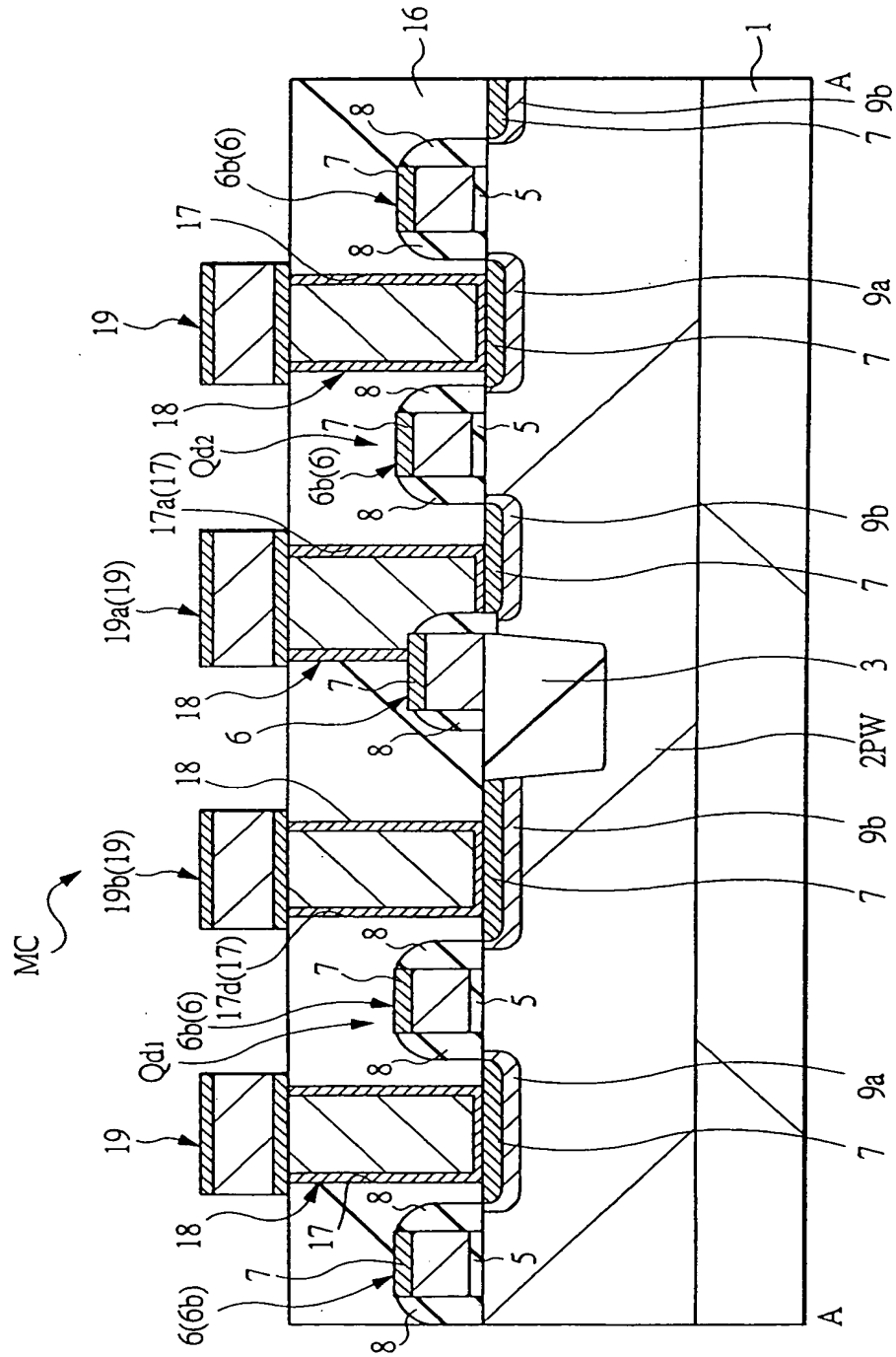
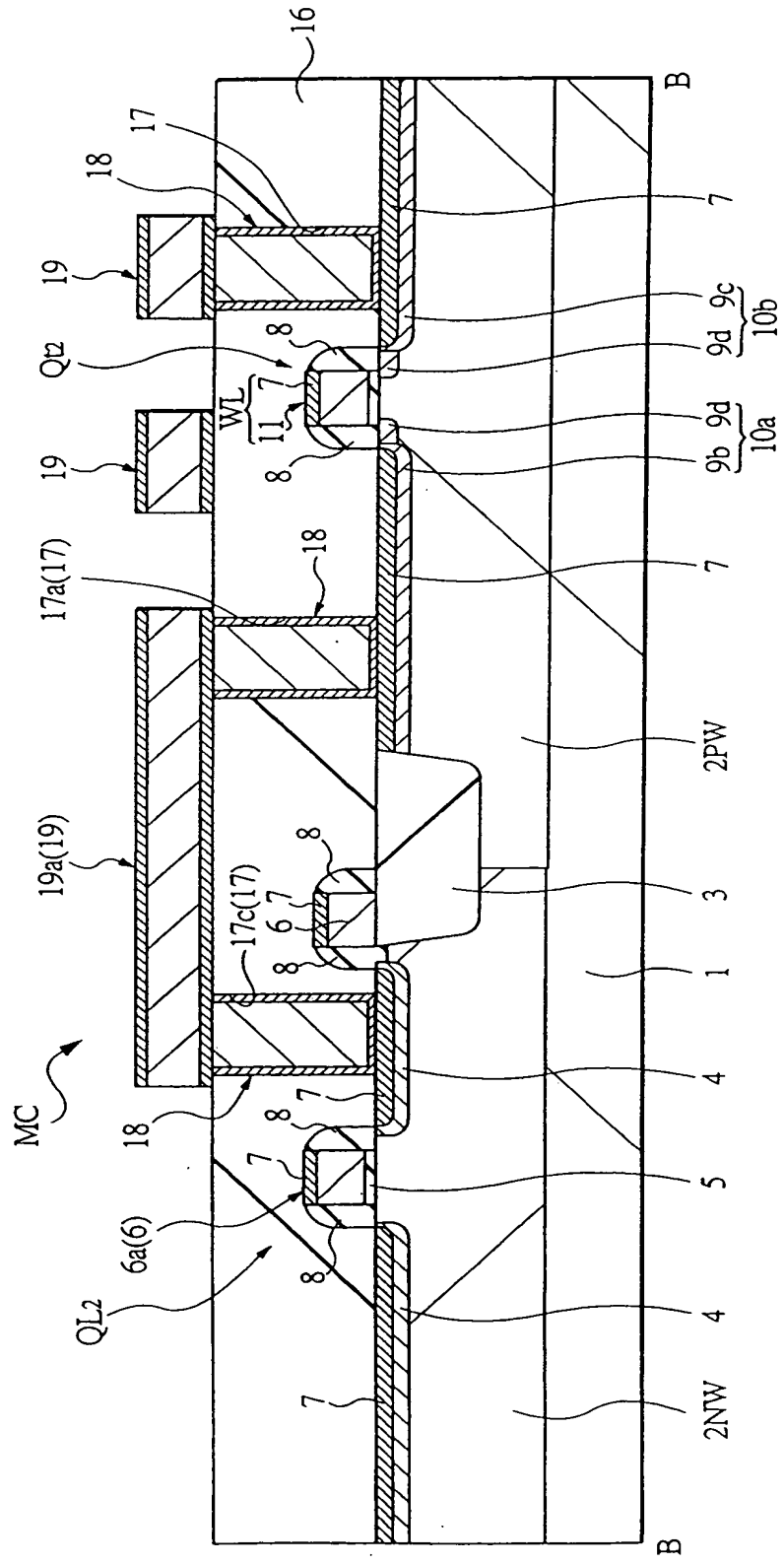
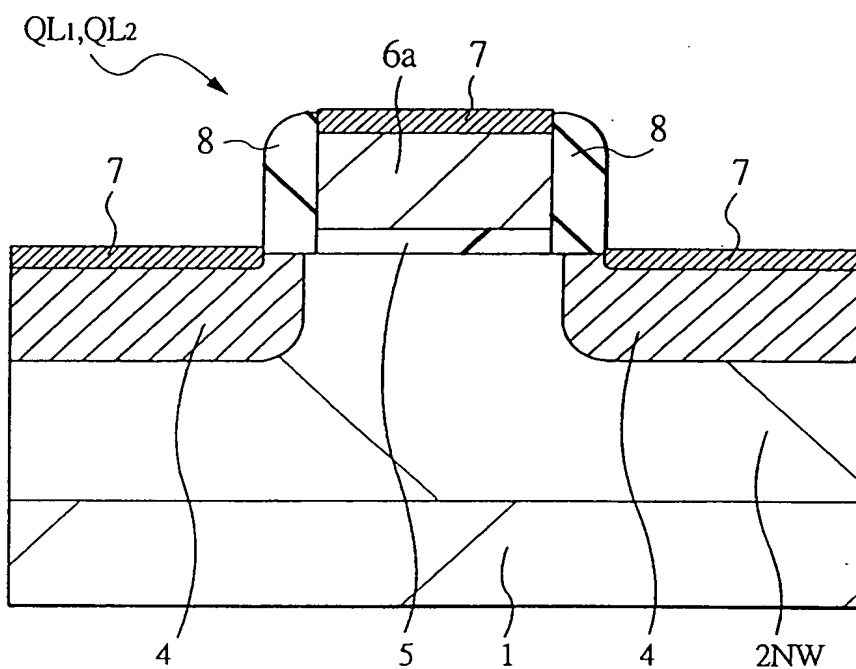


FIG. 16

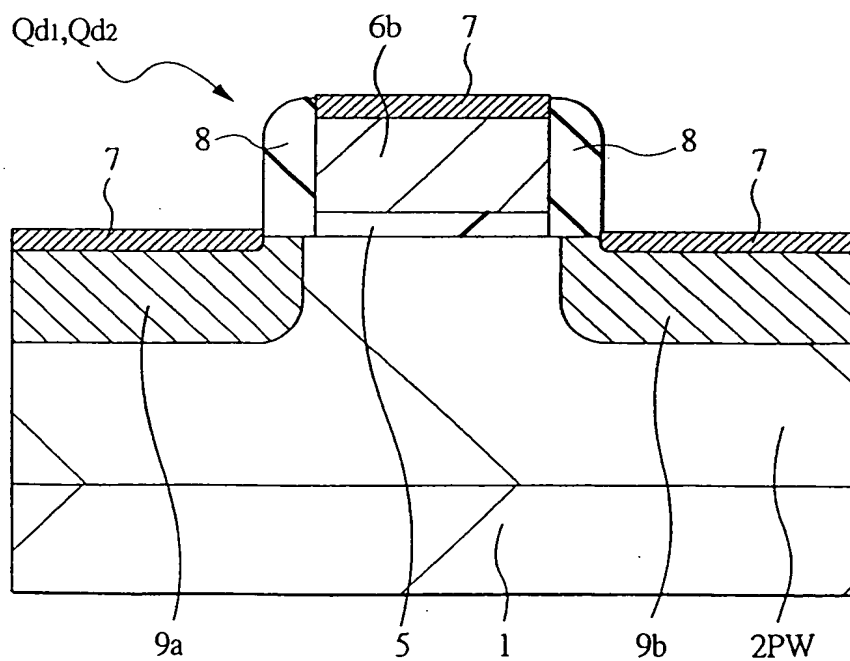




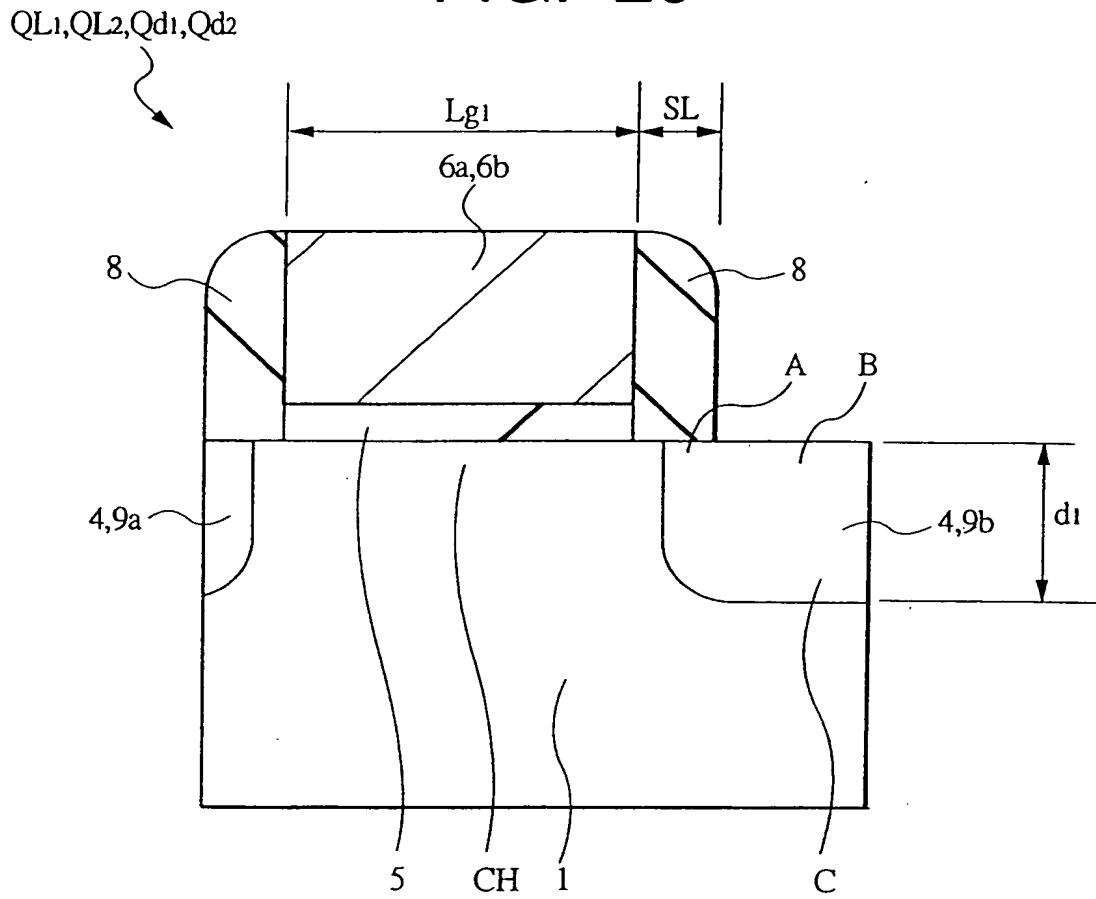
**FIG. 18**



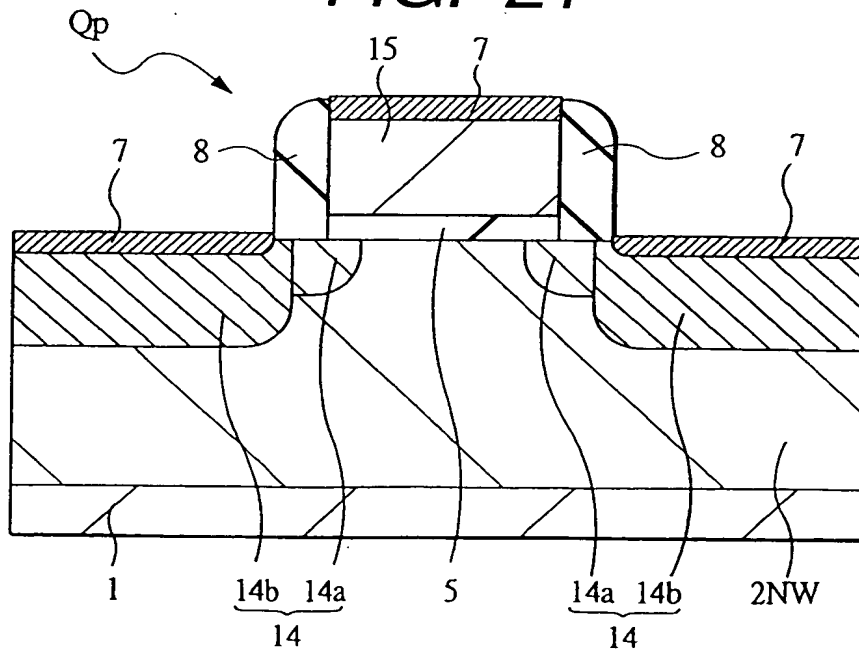
**FIG. 19**



**FIG. 20**



**FIG. 21**



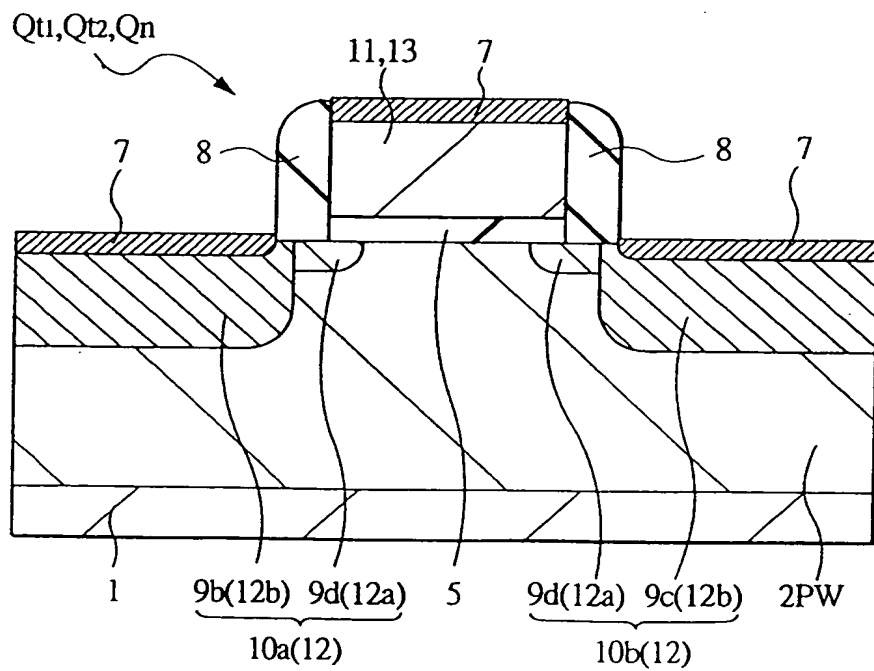




FIG. 24

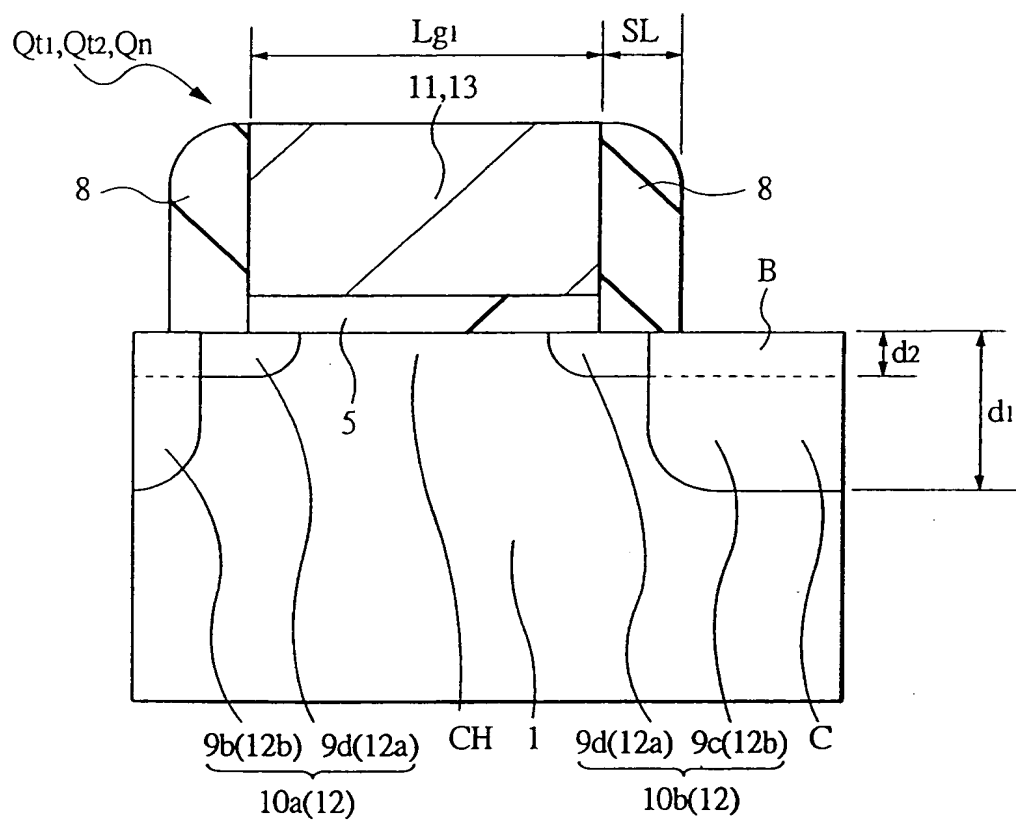


FIG. 25(a)

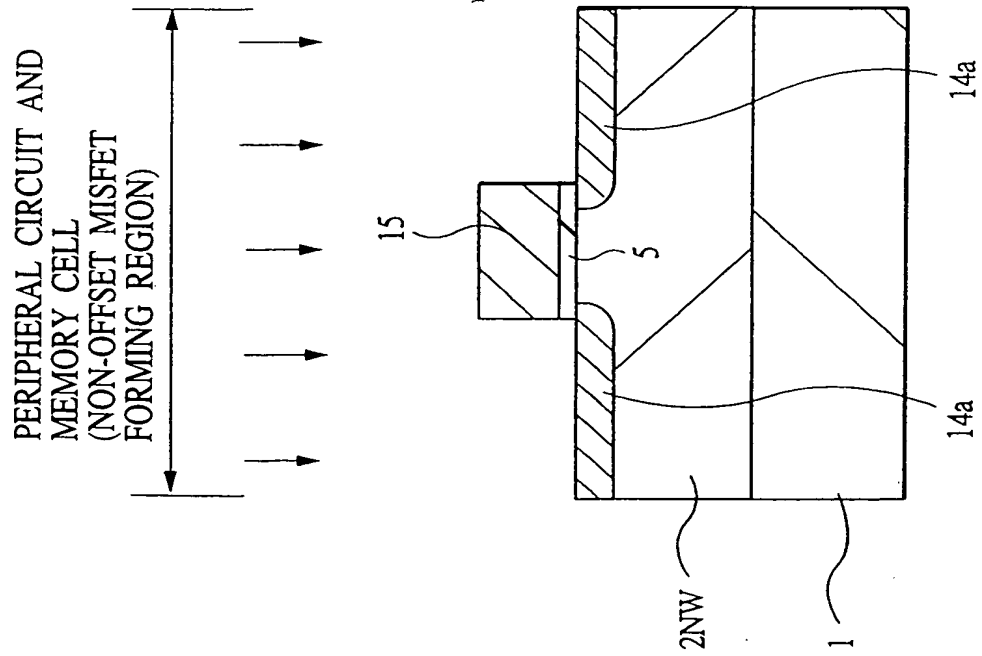


FIG. 25(b)

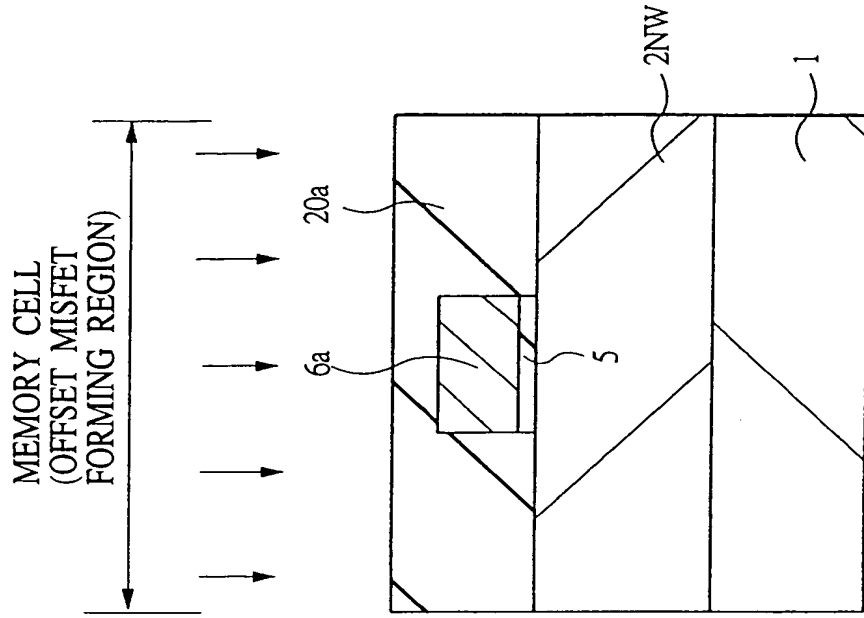


FIG. 26(a)

PERIPHERAL CIRCUIT AND  
MEMORY CELL  
(NON-OFFSET MISFET  
FORMING REGION)

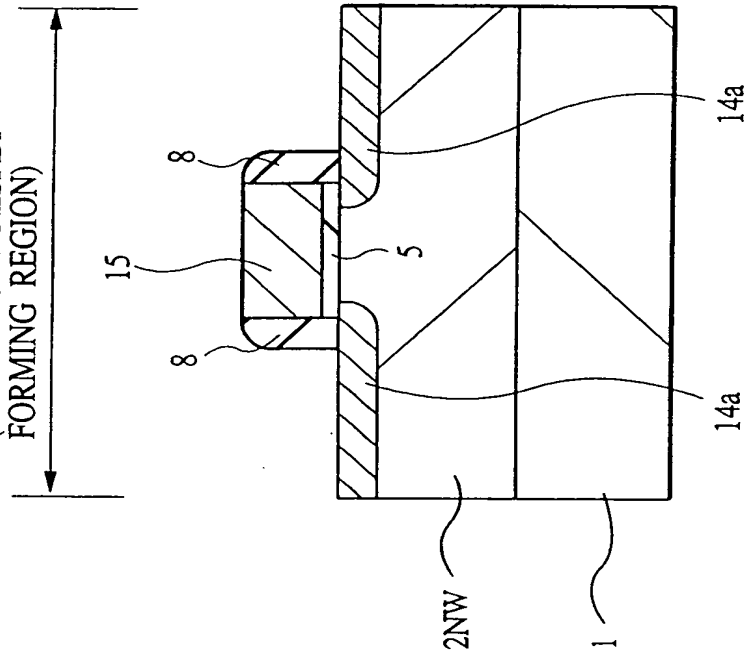
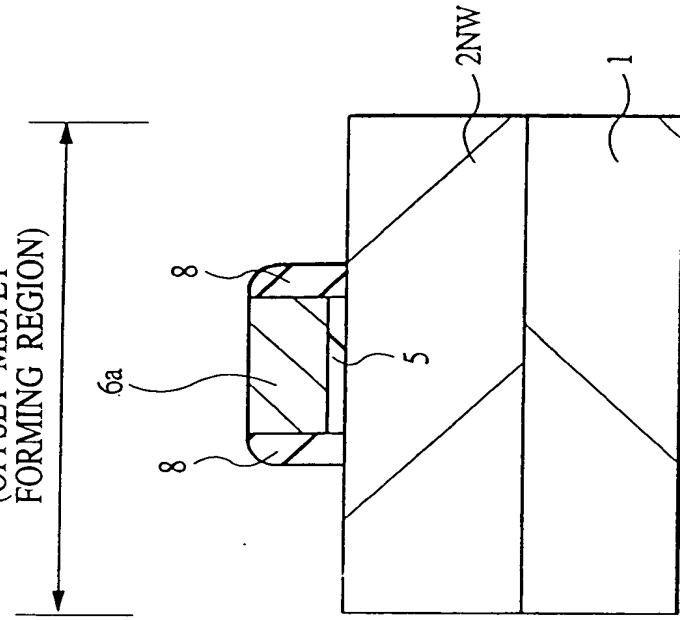


FIG. 26(b)

MEMORY CELL  
(OFFSET MISFET  
FORMING REGION)



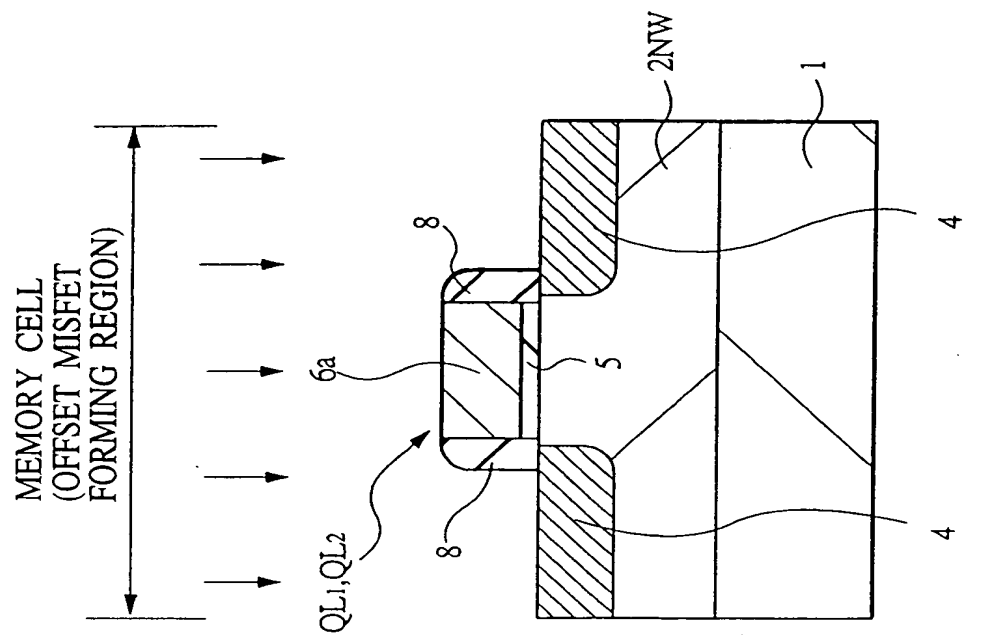
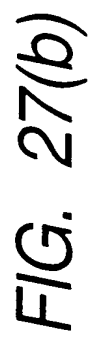


FIG. 28(a)

PERIPHERAL CIRCUIT AND  
MEMORY CELL  
(NON-OFFSET MISFET  
FORMING REGION)

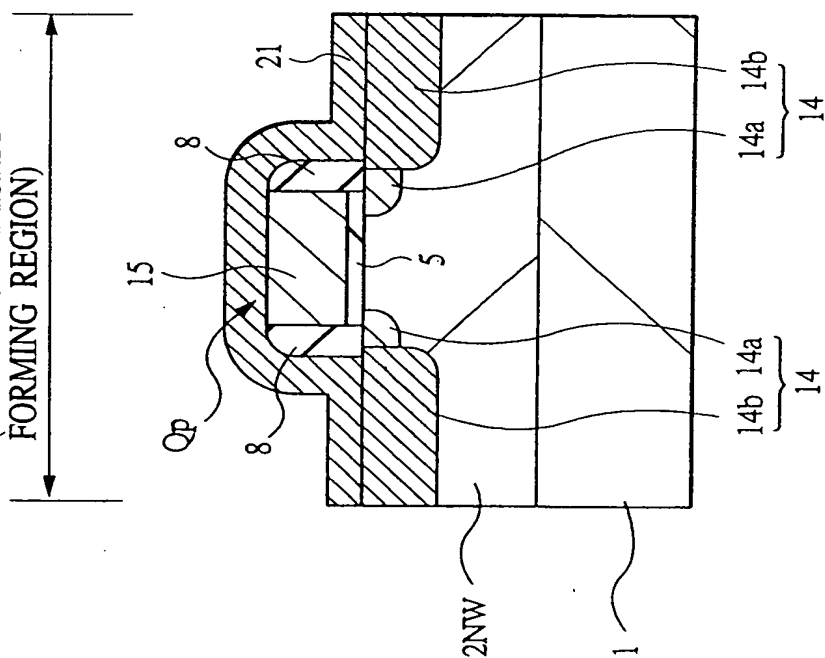
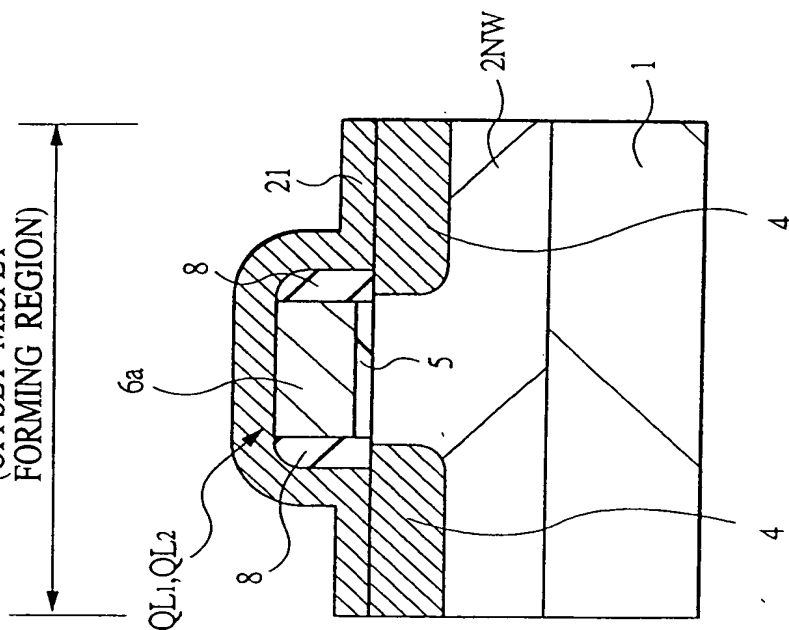
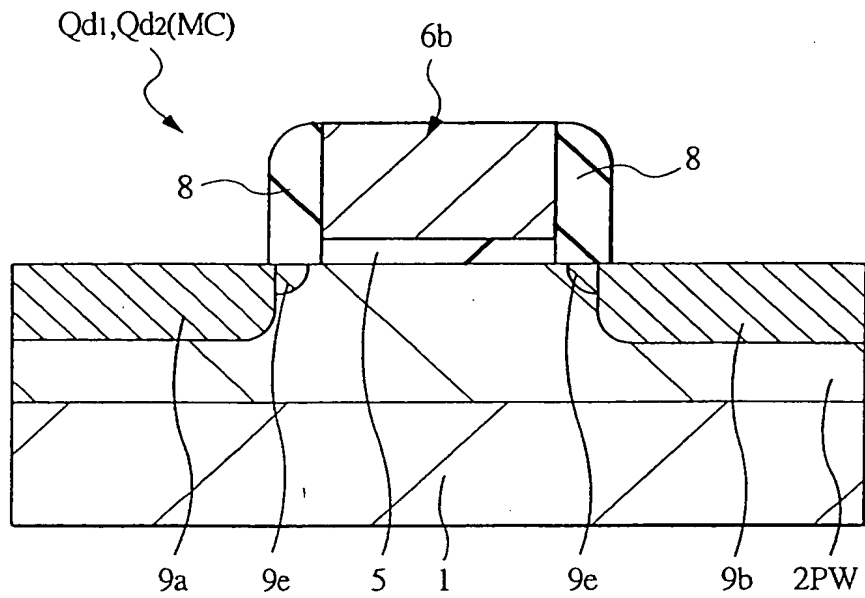


FIG. 28(b)

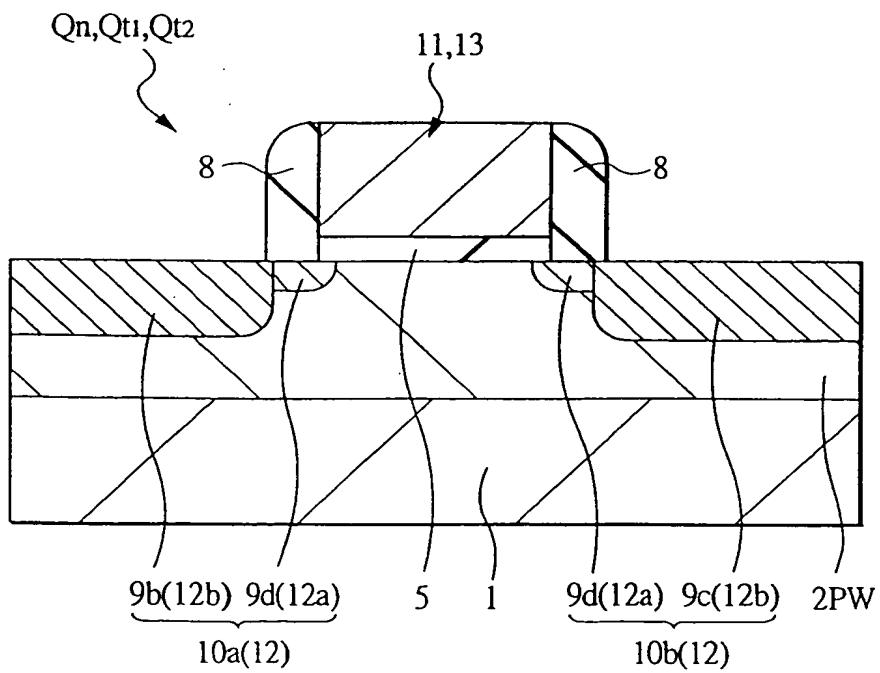
MEMORY CELL  
(OFFSET MISFET  
FORMING REGION)



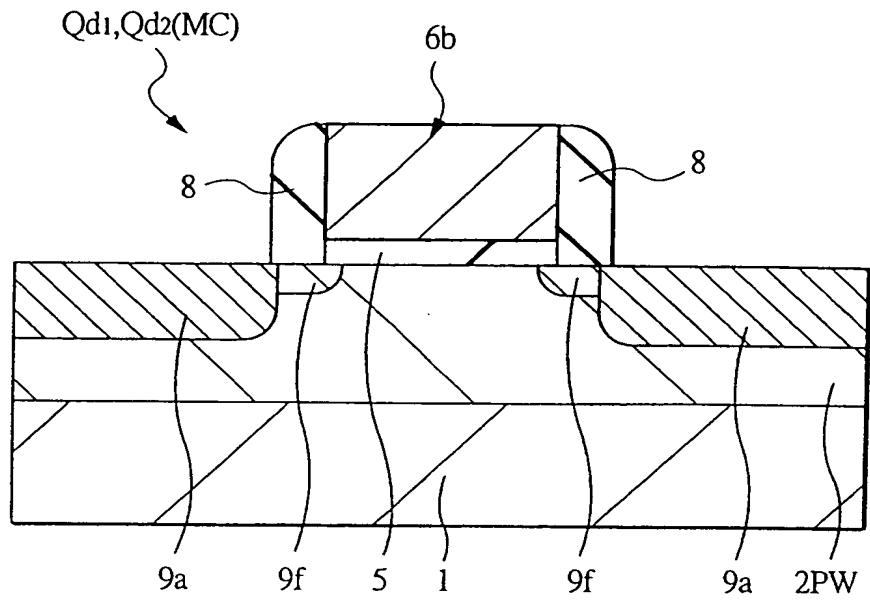
**FIG. 29(a)**



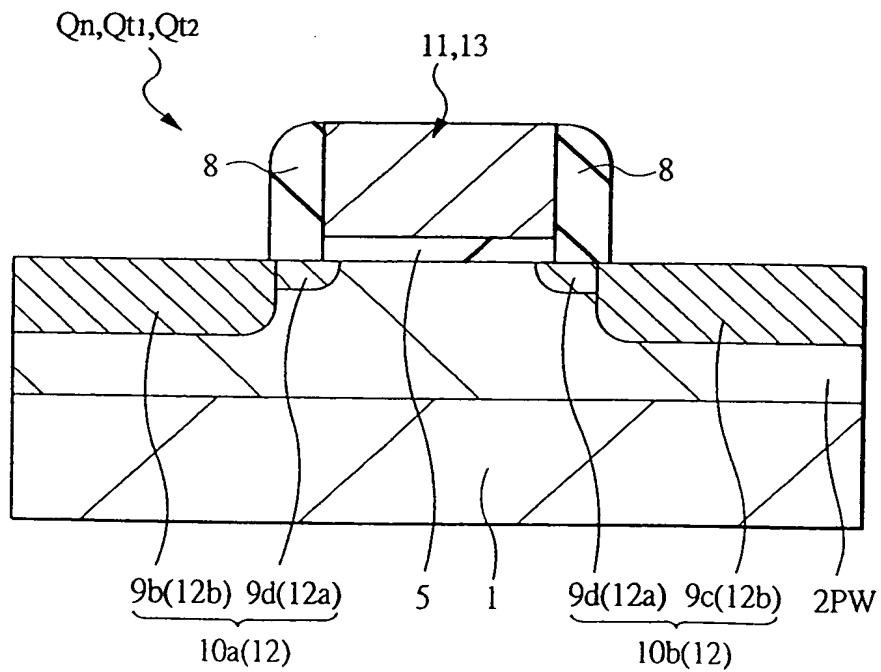
**FIG. 29(b)**



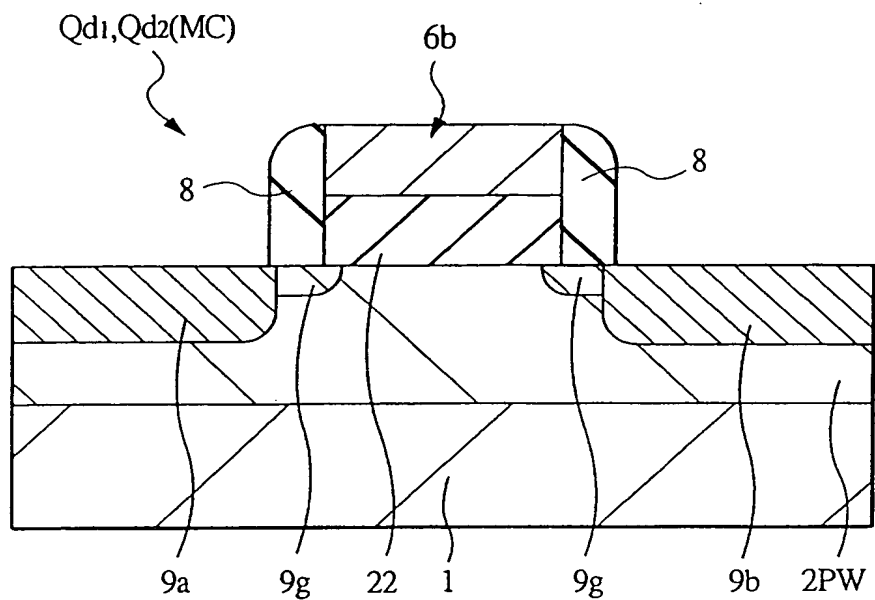
**FIG. 30(a)**



**FIG. 30(b)**



**FIG. 31(a)**



**FIG. 31(b)**

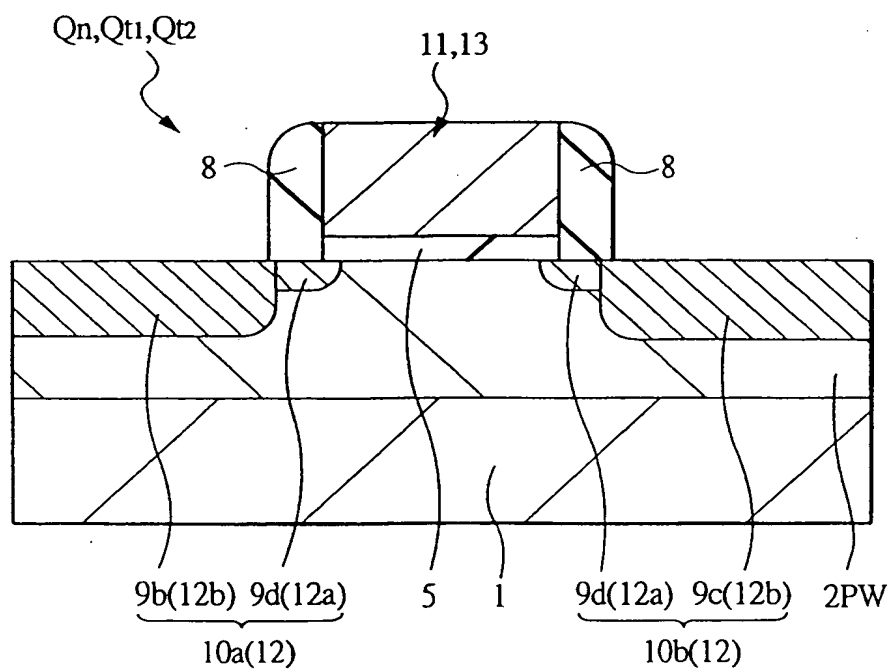




FIG. 32(a)

PERIPHERAL CIRCUIT AND  
MEMORY CELL  
(CONVENTIONAL MISFET  
FORMING REGION)

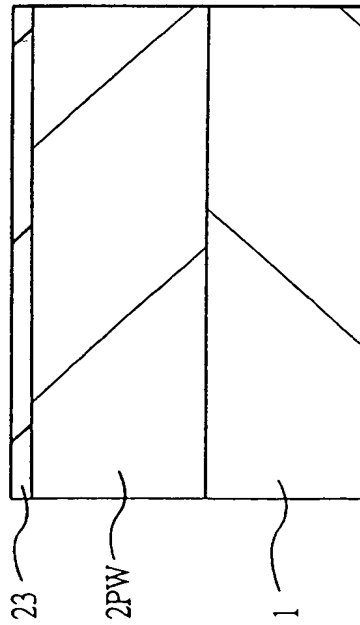


FIG. 32(b)

MEMORY CELL  
(MISFET FORMING REGION  
IMPROVED IN GIDL)

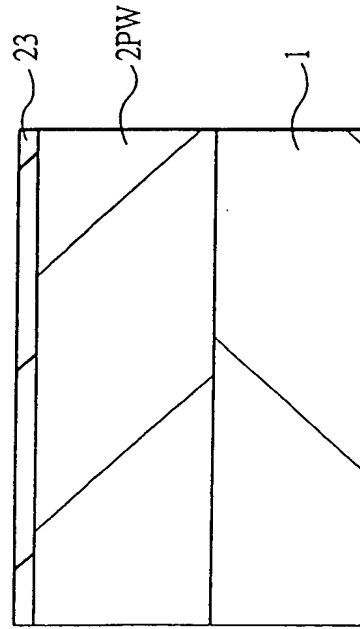
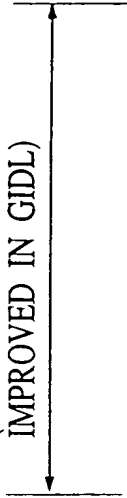


FIG. 33(a)

PERIPHERAL CIRCUIT AND  
MEMORY CELL  
(CONVENTIONAL MISFET  
FORMING REGION)

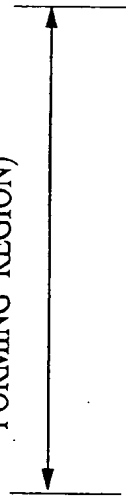


FIG. 33(b)

MEMORY CELL  
(MISFET FORMING REGION  
IMPROVED IN GIDL)

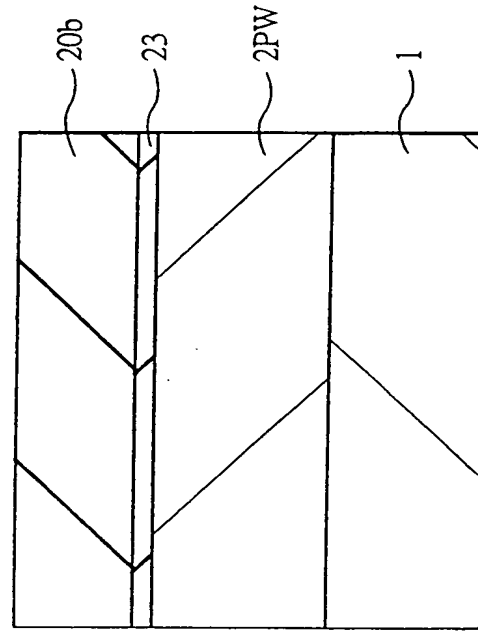
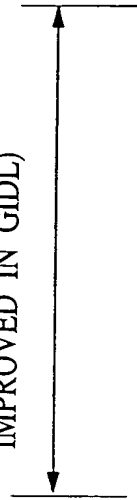


FIG. 34(a)

PERIPHERAL CIRCUIT AND  
MEMORY CELL  
(CONVENTIONAL MISFET  
FORMING REGION)



FIG. 34(b)

MEMORY CELL  
(MISFET FORMING REGION  
IMPROVED IN GIDL)

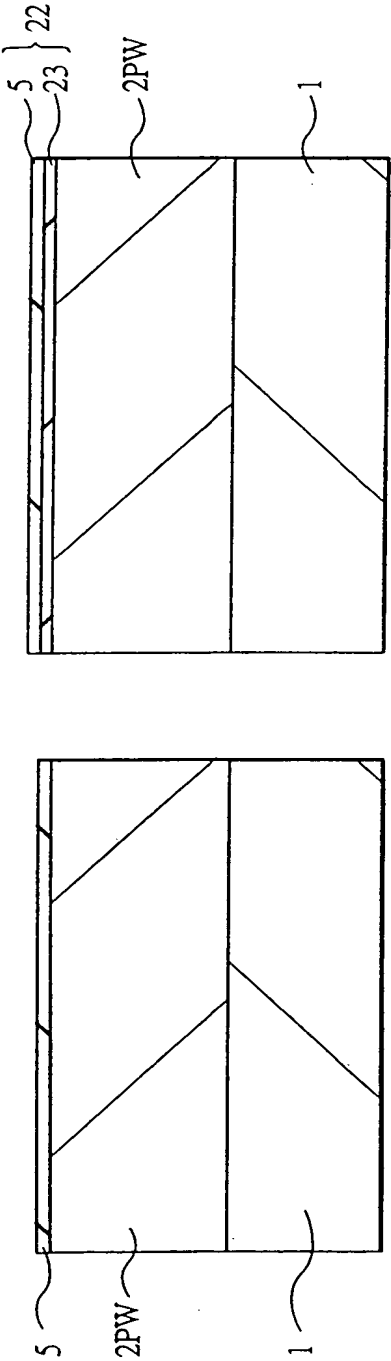
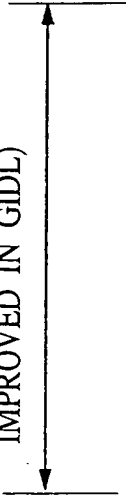


FIG. 35(a)

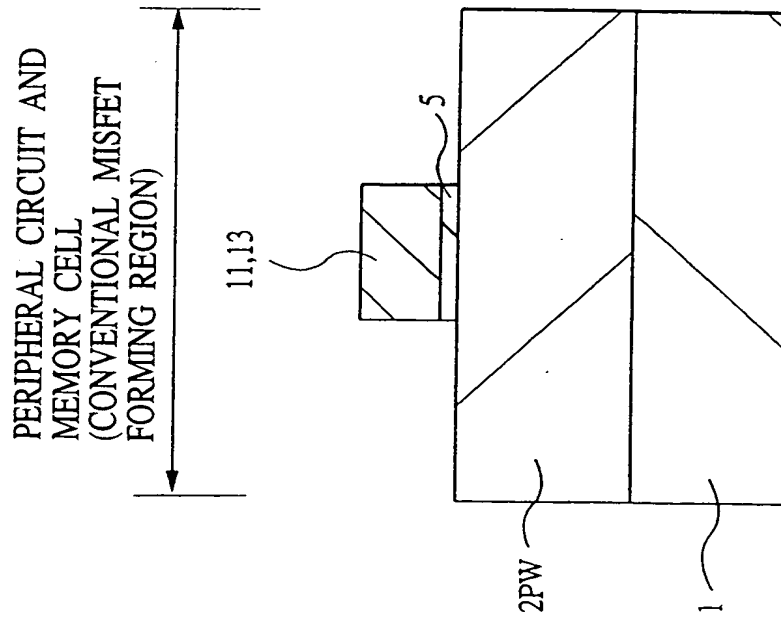


FIG. 35(b)

